Implementation of Novel 2x2 Vedic Multiplier using QCA Technology

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Abstract. Advantages like working at high speed, scalability, and lower power consumption make QCA technology more feasible than modern CMOS technology [1]. QCA Technology uses electrons' Coulombic interaction and polarization to represent binary information 0 and 1. The present paper proposes a novel XOR Gate and a Half Adder design and uses them to implement a novel 2x2 Vedic Multiplier on QCA technology. A 2x2 Vedic Multiplier multiplies two inputs, of two bits each, using Urdhva-Tiryakbhyam Vedic Sutra [2]. The proposed circuit has a reduced cell count and Quantum cost compared to available Co-planar Vedic Multiplier. Open source QCA Designer 2.0.3 is used for the simulation and verification of all three proposed circuits [3].

References:

[1] T. Skotnicki, J. Hutchby, T. King, H.S. Wong, F. Boeuf, The end of CMOS scaling. IEEE Circuits Dev. Mag. **21**(1), 16–26 (2005).

[2] G. K. Ganjikunta, S. I. Khan and M. M. Basha, "A high-performance signed-unsigned multiplier using Vedic mathematics," *Journal of Low Power Electronics*, vol. 15, no. 3, pp. 302–308, 2019.

[3] https://qcadesigner.software.informer.com/2.0/