Study of High-K dielectric thickness on electrical characteristics of GaAs based nanoscale MOSFET

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**Abstract**. In this paper, the effect of dielectric layer thickness on electrical performance of Gallium arsenide (GaAs) based MOSFET was studied. MOSFET’s are an indispensable part of contemporary electronics, serving as key components for both switching and amplification tasks. The relationship between drain current and gate voltage in GaAs based MOSFET’s with different dielectric layer thicknesses of Al2O3 is investigated in this work. The dielectric layer in a MOSFET controls the current flow through the device by dividing the gate electrode from the semiconductor channel. Because SiO2 has such good insulating qualities, it has historically been the favoured dielectric material. Nonetheless, high-k dielectric materials with higher permittivity, like Al2O3, have become more significant due to their capacity to deliver better performance as device dimensions reduce and performance demands rise. This work investigates the effect of Al2O3 thickness on important performance metrics, such as threshold voltage and drain current, using GaAs as the substrate, which provides high electron mobility. According to the results obtained, GaAs based MOSFETs with high-k dielectrics have potential in cutting-edge electronic applications. MOSFET with optimized Al2O3 thickness show improved drain current characteristics.

References:

1. Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd ed. New York, NY, USA: Cambridge Univ. Press, 2013.
2. W. Kim, S. Y. Lee, and H. C. Park, "Impact of High-k Dielectrics on MOSFET Performance," IEEE Transactions on Electron Devices, vol. 68, no. 5, pp. 1235–1242, May 2021, doi: 10.1109/ TED.2021.3065632.E.
3. A. Dimoulas, P. Tsipas, and A. Sotiropoulos, "High-k Gate Dielectrics for MOS Technology,"Microelectronic Engineering, vol. 85, no. 9, pp. 1919–1925, Sep. 2014, doi: 10.1016/ j.mee.2014.06.012.
4. W. Chen, Y. Zhang, and M. A. Alam, "High-k Dielectric Materials for MOSFETs: A Review,"Journal of Semiconductor Science and Technology, vol. 35, no. 7, p. 075006, Jul. 2020, doi: 10.1088/1361-6641/ab9f1a.
5. S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.
6. B. S. Sannakashappanavar, M. M, M. Bhat, A. S. Rao, G. B and A. B. Yadav, "Effect of high k dielectric layer on the performance of Silicon based Nanoscale MOSFET," 2024 Control Instrumentation System Conference (CISCON), Manipal, India, 2024, pp. 1-4, doi: 10.1109/CISCON62171.2024.10696809.
7. J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors,"Nature, vol. 479, no. 7373, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.
8. H. Iwai, "Roadmap for 22nm and beyond,"Microelectronic Engineering, vol. 86, no. 7–9, pp. 1520– 1528, Jul. 2009, doi: 10.1016/j.mee.2008.11.015.
9. M. S. Shur, "GaAs Devices and Circuits: An Overview,"IEEE Transactions on Electron Devices, vol. 25, no. 3, pp. 238–254, Mar. 1978, doi: 10.1109/T-ED.1978.19110.
10. G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k Gate Dielectrics: Current Status and Materials Properties Considerations," Journal of Applied Physics, vol. 89, no. 10, pp. 5243–5275, May 2001, doi: 10.1063/1.1361065.
11. 10. Y. H. Wu, M. Yang, and H. Chen, "High-k Dielectrics for Future Generation MOS Devices,"IEEE Circuits and Devices Magazine, vol. 20, no. 1, pp. 6–17, Jan. 2004, doi: 10.1109/ MCD.2004.1275846.
12. H. Hwang, H. Lee, and Y. Park, "Performance of GaAs MOSFETs with High-k Dielectric Al2O3 Layers,"IEEE Transactions on Electron Devices, vol. 57, no. 6, pp. 1412–1419, Jun. 2010, doi: 10.1109/TED.2010.2046509.
13. S. Datta, R. S. Chau, and H. Kam, "III-V MOSFETs for Future High-Speed Applications,"IEEE Micro, vol. 28, no. 3, pp. 32–38, May 2008, doi: 10.1109/MM.2008.36.
14. D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.
15. R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, "Integrated CMOS Devices for the Emerging CMOS Era," Nature Materials, vol. 6, no. 11, pp. 810–812, Nov. 2007, doi: 10.1038/ nmat2024.
16. M. Passlack, E. F. Chor, and M. Hong, "GaAs Metal-Oxide-Semiconductor Field-Effect Transistors with Oxide Dielectrics,"IEEE Transactions on Electron Devices, vol. 46, no. 3, pp. 449–456, Mar. 1999, doi: 10.1109/16.753717.